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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,553	12/29/2003	Rie Tanaka	16869P-010120US	8456

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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,553	TANAKA ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) 1 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is taken in prosecution of this present application filed December 29, 2003 in which the preliminary amendment has been filed on July 9, 2004. Applicant's arguments and/or amendment have been considered with the results that follow.

2. Claims 2-21 are pending in the Application under examination, as Claim 1 has been canceled.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 3-14 and 18-27 have been considered but not deemed to be persuasive for at least the following.

The claims require "a processor having therein a local memory, the local memory sorting management information relating to data stored in the cache memory". Applicant argued that the applied reference (US 6,356,978 (Kobayashi et al)) fails to teach a processor including a local cache memory storing some part or both the data stored in the cache memory and management information relating to the data stored in a cache memory.

In contrast, the Office Action equates the claimed storage control unit with disk control device (11, in Kobayashi), the disk control unit comprising resource

management units (17a-b), each having respective local cache memory 12a and 12b. While common memory 12a can be considered the claimed cache memory, cache memory 12b is local to resource management unit 17b. While resource management modules 17b updates the management information stored in its own common memory (its local memory) 12b, the same resource management module **17b** simultaneously updates the management information of the common memory (claimed cache memory) 12a provided. Clearly, the features as claimed is anticipated, as Col. 4 (lines 41-46) teaches processor including a local cache memory storing some part or both the data stored in the cache memory and management information relating to the data stored in a cache memory. Col. 5 (Lines 12-20) explains the aspect of local resource and distant resource.

The claims further require "determining if the cache memory can accommodate an operation to write data or to read data". This feature is read as determining whether requested data hits or misses the cache memory. This is a well-known principle of cache memory as cache memory is provided for fast access to local processors while a longer latency period would be required from the same data access in main memory.

The claims further require "identifying additional space require in order to store requested data". Kobayashi additionally teaches identifying vacant or available storage and detecting a fault wherein an area changing means changes a second area into first area [Col. 2, Lines 25-38; Col. 6, Lines 38-61; Col. 12, Lines 43-45].

Per the above-noted remarks the Office rejection with respect to the reference by Kobayashi is maintained and repeated below.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2-21 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,356,978 (Kobayashi et al).

With respect to claims 2, 12, and 16, Kobayashi teaches a system (Fig. 1) comprising a storage control unit ***(disk control device 11)*** and a plurality of storage units ***(disk drive device 103)*** for storing data from a host computer ***(host 102)*** wherein the storage control unit includes: a cache memory (***cache memory 20a, 20b of common memory 12a, 12b)*** for storing data transferred and for storing management information relating to the data stored in the cache memory, and a processor ***(control unit comprising microprocessor 13a, 13b)*** for controlling the storage control unit ***[Col. 4, Lines 54-63]***, the processor having local memory ***(local cache CM 20a, 20b)***, the processor configured to store in its local memory some part of both the data stored in the cache memory and the management information relating to the data stored in the cache memory ***[Col. 4, Lines 41-47; Col. 6, Lines 39-63]***; the processor storing control program for controlling the storage control unit ***[micro-program such as resource sharing program and area determining program) [Col. 3, Lines 52-58; Col. 4, Line***

60 to Col. 5, Line 6] the control program configured to operate the microprocessor to process a read request by performing steps of: accessing the local memory to access the in-memory management information; based on the in-memory management information, determining whether read-out data associated with the read request is stored in the cache memory; if the read-out data is stored in the cache memory, then accessing the cache memory to access the read-out data; if the read-out data is not stored in the cache memory, then: accessing the data storage unit to access the read-out data; storing the read-out data in the cache memory; and updating the in-memory management information and the in-cache management information to indicate an update of the cache memory ***(general principle of cache locality for provided requested data if the data is contained in local cache and if missing the cache, providing the data from external storage, writing back the data in cache and update the management information)*** *[Col. 4, Lines 41-47; Col. 7, Lines 9-51]*. Kobayashi teaches the processor fetches and stores the management information of the cache memory into the memory in the processor ***(Col. 7, Lines 9-16; Col. 7, Lines 32-51)*** the processor updates the management information in the cache memory together with the management information in the processor ***[Col. 4, Lines 41-47; Col. 7, Lines 32-51].***

With respect to claims 3, 6, 19, Kobayashi additionally teaches identifying vacant or available storage and detecting a fault wherein an area changing means changes a

second area into said first area in one of said resource management modules in which a fault is not detected ***[Col. 2, Lines 25-38; Col. 6, Lines 38-61; Col. 12, Lines 43-45]***.

With respect to claims 4-5, 7-11,13-15, 18, and 20-21, Kobayashi teaches: well-known principle of cache memory as cache memory is provided for fast access to local processors while a longer latency period would be required from the same data access in main memory ***[Col. 4, Lines 41-47; Col. 7, Lines 32-51]***; local memory storing some part of data stored and management information for the data stored in the cache wherein the management information includes at least one data attribute for managing the data in the cache memory, a logical address of the data in the cache memory, available storage area information in the cache memory ***[Col. 2, Lines 25-38; Col. 6, Lines 38-61; Col. 12, Lines 43-45]***; the memory in the processor is a volatile memory ***[cache memory or common memory with volatile storage, common feature of processor's memory Col. 12, Lines 31-39]***; the storage units having a RAID configuration, the storage unit comprising magnetic disks ***[plurality of disk drives with disk configuration being of a known principle of disk array, 103, Fig. 1; Col. 12, Lines 40-45]***.

Conclusion

6. Other prior art made of record and not relied upon, but considered pertinent to applicant's disclosure:

US 6,467,029 (Kitayama) teaching data management apparatus and a data management method.

US 6,463,507 (Arimilli et al) teaching layered local cache with lower level cache updating upper and lower level cache directories.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

September 2, 2004